Todor Mladenov Mladenov

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Nationality: Bulgarian
Date of Birth: 17th August 1982

Company: Intel
Position: Senior Member Of Technical Staff: Modem Baseband HW

Office Address:
Intel Deutschland GmbH, AM Campeon 10-12, Neubiberg 85579, Germany

Research Interests

Cellular Baseband, Network on Chip (NoC) and System-on-Chip (SoC) HW Architecture and Design
Coding Theory, Information theory, Estimation theory, MIMO detectors, Pattern matching algorithms
Digital & RF Circuit Analysis, Design and Layout

Experience

Intel, Senior Member of Technical Staff, **Modem Baseband** HW Architecture and Design : April 2017 - Present
Intel, Member of Technical Staff, **SoC and NoC** Architecture and Design: April 2015 – March 2017
Intel, Staff Engineer, **NoC** Architecture and Design: April 2014 – March 2015
Intel, Senior Engineer, **CPU Subsystems** Design: July 2012 – March 2014
Dept. Information and Communications and Dept. of Nanobio Materials and Electronics, GIST – IT Professor with teaching and research focus on Brain Computer Interface (BCI) Systems: May 2011 – June 2012
Communication Sensor Networks Laboratory (CSNL), GIST -Research Assistant : September 2007 – August 2011
Faculty of Engineering, University of New South Wales (UNSW) -Teaching Assistant : May 2009 – July 2009
Communication Systems Laboratory (CSN), GIST -Research Assistant : September 2005 – August 2007
Faculty of Telecommunications, TU-Sofia -Research Assistant : August 2003 – July 2005
Microsoft Bulgaria -Student Consultant for .NET Technology: October 2003 – June 2005
Petrex – ARM Microcontroller Architecture Consultant : September 2004 – May 2005
ECAD Laboratory, TU-Sofia –Internship: Digital Circuit Design Tools: July 2004
Bulgarian Telecommunication Company (Vivacom) –Internship: PC Systems : July 2003
Globaltech Bulgaria -Communication Software Verification : May – July 2002
Radio Communications Laboratory, TU-Sofia –Internship: Analog RF Circuits : January – April 2002

Education

Gwangju Institute of Science and Technology (GIST) *September 2007 – August 2011*
Ph.D., Information and Communications *Final Defense Completed, March 2011*
Dissertation: *Raptor Codes: The Implementation Point of View*
Gwangju Institute of Science and Technology (GIST) *September 2005 – August 2007*
M.Sc., Information and Communications
Thesis: *DDR SDRAM Controller for Embedded Systems*
Technical University of Sofia (TU-Sofia) *September 2001 – July 2005*
B.Eng., Communications and Communications Technologies
Thesis: *Development of Digital System for Mossbauer Analysis*

II English Language School (II AEG), Sofia *September 1996 – June 2001*
High School, Foreign Languages

Skills & Interests

Programming Languages: Assembler, C, C++, Visual C++, Delphi, Matlab, CUDA, OpenCL, TinyOS, Java
Hardware: VHDL, Verilog, ModelSim, PrimeTime, Perl, Verdi, Specman, ICC, Quartus. ADS, PIC & Atmel microcontrollers, ARM and Atom architecture.
Languages: Bulgarian (Mother Tongue), English (5/5), Russian (4/5), German (4/5), Korean (1/5).
Professional Interests: Microprocessor Architecture, Brain Computer interface (BCI) Systems, System on Chip (SoC), Embedded Systems, Digital Circuit Design, VLSI low power circuit design, Computer Architecture, Software Design and Coding, Wireless Communications, GPU Programming, Algorithms.
Hobbies: Swimming, Martial Arts, Mathematics, Ice Skating, Skiing, Electronics, Developing Software, Driving.

Projects (non NDA)

Brain-Computer Interface (BCI) Systems (September 2011 – June 2012)
- Design and implementation of non-medical BCI systems.
- Algorithms and methods for improved real time performance.

Online Computer Assisted Learning (December, 2011 to March 2012)
- Design online learning platform
- Silverlight and ASP.NET technology
- Record, playback, signal processing and visualization of speech

Parallel decoding of fountain codes (March, 2011 to August 2011)
- Design of parallel decoding algorithms.
- Implementation and performance verification on GPU.
- Hardware implementation and performance verification (FPGA, ASIC).

RaptorQ code for MBMS Systems (September, 2010 to January, 2011)
- Implementation and evaluation on workstation and embedded system.
- Design of efficient decoding algorithm.
- Implementation and verification on FPGA.

Raptor codes on binary erasure channel (BEC) (August, 2008 to May,2010)
- Performance evaluation on NIOS II embedded system.
- Parallel scalable hardware architecture for Raptor decoder.
- Hardware/Software co-design of Raptor decoder.
- Design of incremental decoding algorithms
- Implementation and verification on FPGA

SHA-2 hardware intellectual property (IP) (March, 2008 to May, 2008)
- Design of energy efficient hardware architecture.
- Implementation and verification on FPGA.

DDR SDRAM Controller IP (March, 2007 to July, 2007)
- Design of energy efficient hardware architecture for video.
- Implementation and verification on FPGA.

MMIC Voltage controlled oscillator (VCO) at 26 GHz (October, 2005 to November, 2005)
- Design and Implementation with commercial foundry library.

MPEG 2 Video codec (September, 2005 to February, 2007)
- Hardware architecture of H.263 and H.222 standards.
- Implementation and verification on FPGA.

Digital Module for Mossbauer Spectral Analyzer (September, 2003 to July, 2005)
- Design of printed circuit board (PCB).
- Design and coding of PC user application.

- Design and coding of microcontroller application.
- Design, implementation and verification of digital circuits on CPLD.

Lectures

Embedded Systems Design, Spring Semester 2011, GIST, Dept. Information & Communications
Brain-Computer Interface (BCI) Systems, Spring Semester 2012, GIST, Dept. information & Communications and Dept. of Nanobio Materials and Electronics

Patents

"Interconnect Networks Supporting Multiple Consistency Mechanisms, Multiple Protocols, and Multiple Switching Mechanism", 2016: https://patents.justia.com/patent/20180165240
"Control and Data Multiplexing", 2017: https://patents.justia.com/patent/20180375602
"Trace Network used as a Configuration Network", 2017: https://patents.justia.com/patent/20190089582

Journal Publications

Linjia Hu, Saeid Nooshabadi, **Todor Mladenov**, "Forward error correction with Raptor GF(2) and GF(256) codes on GPU", IEEE Trans. Consumer Electronics 59(1), pp. 273-280 (2013)
T. Mladenov, S. Nooshabadi, Juan A. Montiel-Nelson and K. Kim, "*Decoding of Raptor Codes on Embedded Systems*", Elsevier Microprocessors and Microsystems - Embedded Hardware Design (MICPRO), pp. 375-382, Vol. 36, Issue 5, July 2012.
T. Mladenov, S. Nooshabadi, and K. Kim, "*Efficient GF(256) Raptor Code Decoding for Multimedia Broadcast/Multicast Services and Consumer Terminals*," IEEE Trans. on Cons. Electron.,pp. 356-363, Vol. 58, Issue 2, May 2012.
T. Mladenov, S. Nooshabadi, and K. Kim, "*Efficient Incremental Raptor Decoding over BEC for 3GPP MBMS and DVB IP-Datacast Services*," IEEE Trans. on Broad., Vol. 57, No.2, pp.313-318, June 2011.
T. Mladenov, S. Nooshabadi, and K. Kim, "*Implementation and Evaluation of Raptor Codes on Embedded Systems*," IEEE Trans. on Comp., Vol. 60, No. 12, pp. 1678-1691, December 2011.
T. Mladenov, S. Nooshabadi, and K. Kim, "*MBMS Raptor Codes Design Trade-offs for IPTV*," IEEE Trans. on Cons. Electron., vol. 56, no. 3, August 2010.
T. Mladenov, S. Nooshabadi, and K. Kim, "*Strategies for the Design of Raptor Decoding in Broadcast/Multicast Delivery Systems*," IEEE Trans. on Cons. Electron., vol. 56, no. 2, pp. 423-428, May 2010.
T. Mladenov, S. Nooshabadi, and K. Kim, "*Hardware Accelerator for Raptor Decoder*," International Scientific and Applied Science Conference ELECTRONICS 2009, published in Ann. Journal of Electr., Issue 1, Vol. 3, pp. 64-67

Conference Publications

T. Mladenov, "5G Pdsch Front End Distributed Control HW processor Architecture", DTTC, 2019
H. Tajouri, **T. Mladenov**, "Analytical Modeling of Network on Chip", IETC, November 2015
H. Reining, **T. Mladenov**, S. Bernardi, J. Hermann, R. De Gruijl, K. Nair, B. Klein, „Mobile NoC Fabric For Low Cost Mobile Devices", IETC, November 2014
L. Hu, S. Nooshabadi, **T. Mladenov**, "Forward error correction with RaptorQ code on GPU", ISCAS 2013, pp. 281-284
T. Mladenov, S. Nooshabadi, and K. Kim, "Accurate Motor Imagery Based Dry Electrode Brain-Computer Interface System for Consumer Applications," in Proc. of IEEE 16th International Symposium on Consumer Electronics (ISCE), pp. 1-4, June 2012
R. Babaei, **T. Mladenov**, and K. Kim, "Reducing the False Detection Rate of Hand Motor Imagery Based Dry Electrode Brain-Computer Interface System," in Proc. of GIST 2012 Health Conference, May 2012
Philipp M. Eittenberger, **T. Mladenov,** and Udo R. Krieger, "*Raptor Codes for P2P Streaming,"* in Proc. of Euromicro International Conference on Parallel, Distributed and Network-Based Processing (PDP), pp. 327 - 332, Feb. 2012
T. Mladenov, S. Nooshabadi, and K. Kim, "*Forward Error Correction with RaptorQ Code on Embedded*

Systems," in Proc. of IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), August 2011

T. Mladenov, S. Nooshabadi, Juan A. Montiel-Nelson and K. Kim, "*Implementation and Performance Evaluation of Raptor Codes on Embedded System*," in Proc. of XXV Conference on design of Circuits and Integrated Systems (DCIC), Lanzarote, November 2010

T. Mladenov, S. Nooshabadi, K. Kim, and A. Dassatti, "*Analysis and Implementation of Raptor Codes on Embedded System*," in Proc. of IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 45-48, August 2010

T. Mladenov, S. Nooshabadi, K. Kim, and A. Dassatti, "*Parallel Scalable Hardware Architecture for Hard Raptor Decoder*," in Proc. of IEEE International Symposium on Circuits and Systems (ISCAS), pp. 3741-3744, May 2010

T. Mladenov, S. Nooshabadi, K. Kim, and A. Dassatti, "*Hardware Implementation of Matrix Inversion for Raptor Decoder on Embedded System*," in Proc. of IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 678-690 ,August 2009

T. Mladenov, and S. Nooshabadi, "*Implementation of Reconfigurable SHA-2 Hardware Core*," in Proc. of IEEE Asia Pacific Conference on Circuits and Systems, pp. 1802-1805, 2008

T. Mladenov, F. Mujahid, E. Jung, and D. Har, "*Bandwidth, Area Efficient and Target Device Independent DDR SDRAM Controller*," in Proc. of XVIII International Conference on Computer and Information Science and Engineering (CISE), Vol. 18, pp. 102-106, Vienna, Austria, 2006

T. Mladenov, F. Mujahid, E. Jung, and D. Har, "*Implementation of High Data Rate Stream Parsing with Data Aligning Mechanis*m," in Proc. of IEEE International Symposium on Signal Processing and Information Technology (ISSPIT), pp. 697-701, Vancouver, Canada, 2006

T. Mladenov, and V. Mladenov, "*Interface Module for Mossbauer spectral Analysis*," in Proc. of International Scientific and Applied Science Conference ELECTRONICS, Sozopol, Bulgaria, 2005

V. Mladenov, and **T. Mladenov**, "*Reconfigurable Controller for Industrial Applications*," in Proc. of International Scientific Conference "COMPUTER SCIENCE", Sofia, Bulgaria, 2004

T. Mladenov, and V. Mladenov, "*Microcontrollers' Programmer*," in Proc. of International Scientific and Applied Science Conference ELECTRONICS, Sozopol, Bulgaria, 2004

Students Supervision

- Safaiya Raiyan: Master's Thesis, TU Dresden
- Hela Tajouri: Master's Thesis, TU Munich
- Nicolai Oswald: Master's Thesis, TU Munich
- Kai Mast: Bachelor's Thesis, University of Bamberg
- Linus Dietz: Bachelor's Thesis, University of Bamberg
- Miroslav Mihalev: Internship, TU Sofia
- Anastasios Psarras: Ph.D. Internship, Democritus University of Thrace
- Ioannis Seitanidis: Ph.D. Internship, Democritus University of Thrace

Awards & Scholarships

- **Doosan Research Scholarship** for excellent research record in 2009-2010 period
- **National IT Industry Promotion Agency of Korea**, Scholarship, September 2007 - August 2011
- **Korean Research Foundation**, Scholarship, September 2005 - August 2007
- **Technical University of Sofia**, Scholarship, January 2004 - July 2005

Reference(s) available upon request!

Prof. Kiseon Kim, Gwangju Institute of Science and Technology (GIST), email: kskim@gist.ac.kr
Prof. Saeid Nooshabadi, Michigan Technological University (MTU), email: saeid@mtu.edu
Prof. Angel Popov, Technical University of Sofia (TU-Sofia), email: anp@tu-sofia.bg
Dr. Helmut Reinig, PE at Intel Corporation, email: helmut.reinig@intel.com
Simona Bernardi, Sr. Staff member at Intel, email: simona.bernardi@intel.com
Frank Pitter, Group Manager at Intel, email: frank.pitter@intel.com